1/4 W Optical Receiver and Clock Recovery Circuit for Gb/s Digital Fiberoptic Links

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ABSTRACT

Design and simulation of a low power consuming MMIC chip set is presented in this paper, which is used as an optical receiver and clock recovery circuit operating up to 1.25Gb/s. This design is based on BTA24 Si BJT transistor array from Bipolarics. Major design innovations such as push-pull self-oscillating mixer and a push-push frequency doubler is used to provide a total power consumption of 247mW in an area of only 700μmx700μm.

INTRODUCTION

In the last few years, state-of-the-art of fiber optic links has gone through enormous evolution and low loss, high-speed digital fiber optic links have been realized in modular forms. Fundamental components of digital fiber optic distribution networks are data source (modem), optical transmitter (either laser diode or LED based), fiber optic distribution network, optical receiver, clock recovery circuit and decision making circuit. With availability of high-speed optical sources and photodetectors, the focus is now in the development of an integrated opto-electronic circuit, which is low power consuming. The conventional clock recovery schemes needs to be re-evaluated to meet the low power consumption requirements.

The design of the integrated optical receiver and clock recovery circuit is based on Si BJT from Bipolarics (BTA24) and follows the block diagram shown in Fig. 1. In this diagram an optical receiver detects data signals at 1.25Gb/s from a modulated optical signal, received from the fiber optic distribution networks. The detected signal is amplified using a trans-impedance amplifier, and then provided to the decision and clock recovery circuit. The output of the clock recovery circuit at 1.25 GHz is also inputted to the decision circuit to regenerate the data signal. The goal of this paper is to present an integrated optical receiver and clock recovery circuit for detection of 8B10B NRZ data signals at 1.25Gb/s.

DESIGN APPROACH

The optical receiver is realized using a PIN photodiode and a trans-impedance amplifier, as presented last year [1]. A high sensitivity is predicted up to frequency of 1.25GHz with a power consumption of 137mW. The clock recovery circuit is designed based on the principle of ILPLL technique [2]. The 8B10B NRZ data stream at 1.25Gb/s rate has a frequency line spectrum at 625 MHz, which is filtered and injected to an ILPLL push-pull clock recovery circuit (cf. Fig. 1). This approach is selected over all other competitive techniques [3-6] because of the combined functions of injection locking and phase locking provides a larger tracking range, shorter pull-in time, and a smaller power consumption than the conventional PLL techniques. Furthermore, in order to reduce the electrical power consumption of the ILPLL design, a push-pull self-oscillating mixer [7] design topology is advocated to combine the oscillation and phase detection blocks in [1]. A push-pull operation provides a low power consumption and efficient mixing.

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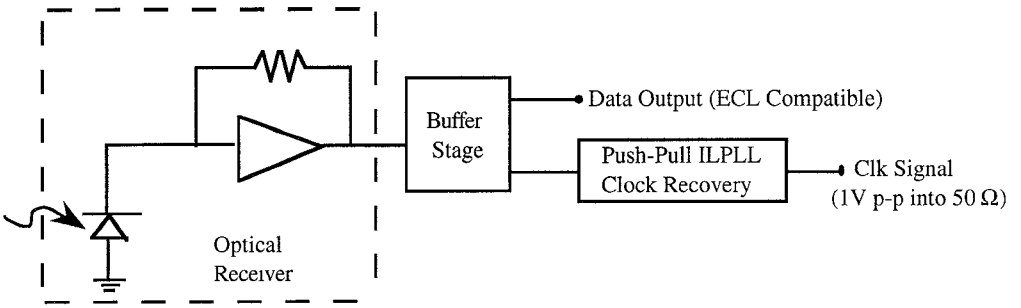

Fig. 1 Block diagram of the low power consuming optical receiver and clock recovery circuit.

The designed circuit utilizes ten BJTs (vs. 17 in [1]), as shown in Fig. 2. The 625 MHz oscillation is based on Colpitts oscillator design, however the gain block is provided by transistors Q1 and Q2, as a differential pair Class AB amplifier. The amplified signal is fedback through an external resonant tank circuit (a tunable resonator at 625MHz). The feedback function is provided by the two resistors, Rf, which sample the collector current in one transistor and feed it back to another transistor as the base voltage. Each transistor only has a DC collector current of 3 mA to maintain a low power consumption with enough gain. On the other hand, one may achieve a very large voltage swing between the two collector by using large value of resistors at collector. The large voltage swing is the key characteristics required from the oscillator to drive the self-oscillating mixer and perform frequency doubling function. The phase and frequency stabilization is achieved using the 625 MHz spectral line of the data signal (cf. Fig. 1). The reference signal for injection locking and the phase reference for phase locking are in quadrature for efficient phase error detection. Phase comparison with the phase reference signal is conducted in transistor Q3, and the error signal is amplified by the differential amplifier Q8, Q9 and Q10 and then applied to the varactor diode in the tank circuit.

The output of the ILPLL push-pull oscillator is inputted to a push-push frequency doubler, as shown in Fig. 2. The Class AB transistors allow the positive portion of the base voltages in Q4 and Q5 to pass through. In this design, one transistor remains at "off" state during a negative half cycle, while the other is "on". This circuit adjusts the DC current automatically to be exactly 50% of the total current swing according to the output power. Note DC blocking capacitors are avoided in the emitter follower design. To achieve a clock signal with 1V peak to peak swing, a minimum 2 V input voltage is then required. This requirement is easily satisfied because of the large load resistance of Q1 and Q2, which provides large voltage swing of up to 3 V under the condition of Vcc=5 V. The transistor Q6 is then used to power amplify the clock signal in order to drive the ECL compatible decision circuit. Biasing Q6 at 10 mA satisfies the required a clock frequency current swing of 20 mA to a 50 Ω load at 1.25GHz. Transistor Q7 is used to adjust the collector current exactly at 10 mA, thus preventing the DC power consumption.

SIMULATION RESULTS

The simulation of this circuit was performed using MW-SPICE. The Spice parameters are used in simulation of B12V105 NPN bipolar transistor from Bipolarics. Fig. 3 depicts time evolution of the collector current in transistor Q1. A steady oscillation is obtained quickly after 70nS of turning DC power on. The current swing is about 7 mA and the DC current of this transistor is only 3.5 mA. Observing the voltage wave-form between the two collectors of Q1 and Q2 in a zoomed region of 8 nS indicates the oscillation frequency of about 625 MHz. Simulations also indicates efficient mixing in the push-pull self-oscillating mixer. The down converted phase error signal could tune the Colpitts oscillator over 100MHz around 625MHz. The simulations results of the frequency doubler is shown in Fig. 4. The rejection of fundamental frequency is nearly ideal because of the symmetry of the input wave-form at Q4 and Q5. A clock signal at 1.25 GHz is observed with a 1V swing on a 50Ω load.

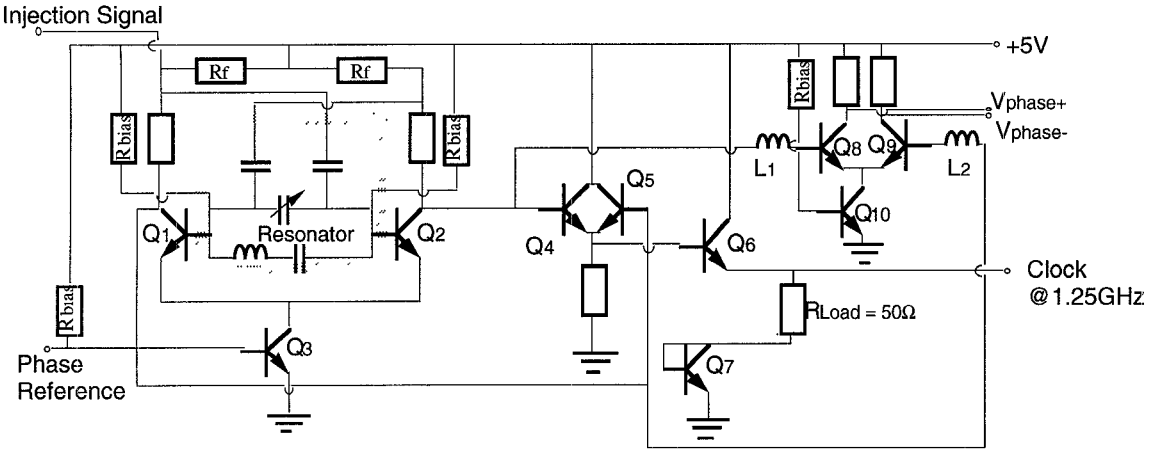

Fig. 2. The schematic diagram of the designed multi-function MMIC circuit.

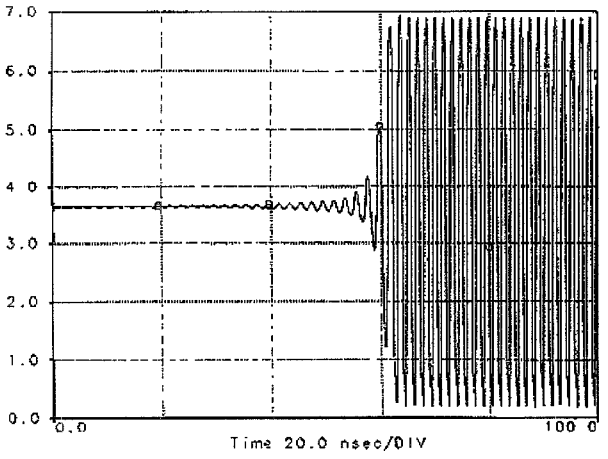

Fig. 3. Collector current of the transistor Q1, indicating start of the oscillation process. (Vertical axis is collector current in mA and horizontal axis is time in 20ns/div.)

MMIC LAYOUT

The clock recovery design are laid out using BTA24 transistor array of Bipolarics, which employs the 0.7μm BJT transistors [1]. A total of only 13 transistors is required for the optical receiver/clock recovery circuit, thus it is convenient to integrate the whole circuit on one BTA24 chip set. This circuit is laid out using the Bipolarics design rules and the full realization of this MMIC is shown in Fig. 5. "**Vin**" contact pad is used for the incoming signal from a PIN photodiode, whereas "**TZA out**" contact pad provides the output from the trans-impedance amplifier (TZA). This output is shared by the decision circuit and the resonant tank circuit of 625MHz, which precedes the push-pull ILPLL clock recovery circuit. The output of the frequency doubled signal is retrieved from the "**FDout**" contact pad and is provided to a 50Ω load. The chip size is only 700μmx700μm. There are only 18 bonding pads for input/output interconnection; therefore SSOP-20, a low cost surface mount type plastic package, is selected for packaging this MMIC chip-set.

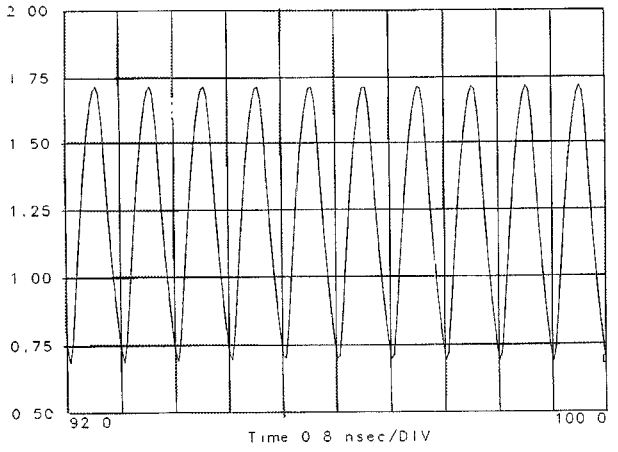

Fig. 4. The extracted clock voltage signal at 1.25GHz at a 50Ω termination. (Vertical axis is output voltage in V and the horizontal axis is 0.8 ns/div.)

CONCLUSIONS

This designed optical receiver and clock recovery circuit requires very small prime power of ≤1/4W. A significant reduction in the power consumption is achieved by replacing separate ooscillator, mixer and doubler to a push-pull self-oscillating mixer and a push-push frequency doubler (only 110mW as compared to 490mW in [1]). This designed chip-set, with different external lumped elements is very attractive for the fiber optic based local area distribution networks used in aircrafts from 140Mb/s up to 2.5Gb/s.

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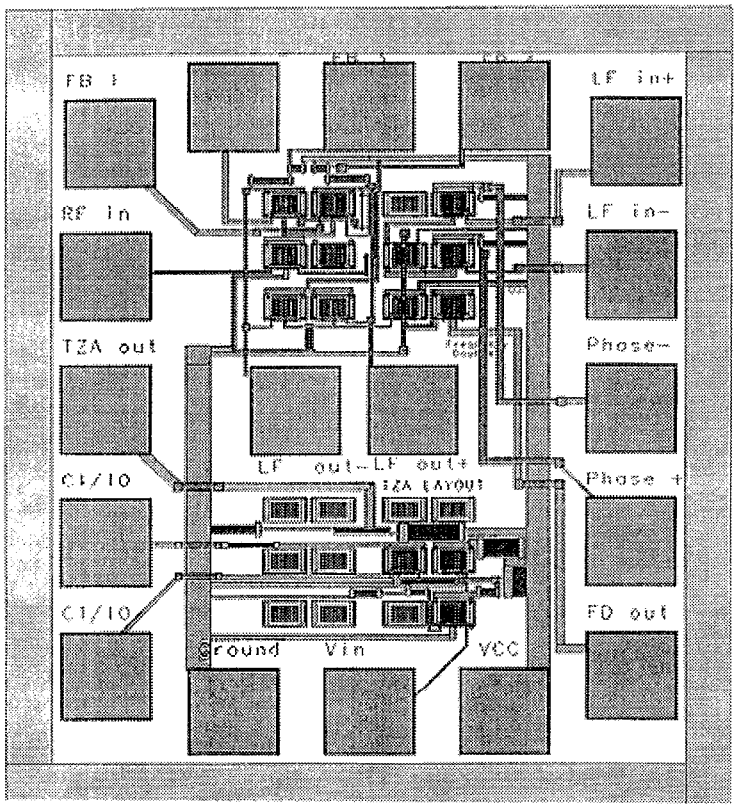

Fig. 5. MMIC layout of the 1.25Gb/s optical receiver and clock recovery circuit designed for BTA24 Si BJT array, available from Bipolarics.